

DETAILED ACTION

This detailed action is in regards to United States Patent Application 11/722,509 filed on 11/28/2003 and is a first action based on the merits of the application.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 11-15 and 17-22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 11recites a programmable gain levels for providing a plurality of gain defined by $G_n=G_1 \cdot K^n$. G_n and G_1 are undefined in the claims and it is unclear what is represented by the variables. While the specification is read in light of the specification limitations from the specification cannot be read into the claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 2 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Addiss (US 5,623,938) in view of Bookspan (US 5,086,781)

Addiss teaches a system for detecting the possibility of disease in one of a first body part and a second substantially similar body part by impedance measurements, the system comprising: b) a front-end module (electrodes 12 and 14) connected to the main module and at least one of the first and second body parts (P) for injecting

stimulus currents into the at least one of the first and second body parts and receiving voltages generated by the at least one of the first and second body parts in response to the stimulus currents; and, c) an impedance module connected to the main module and the front-end module for creating the stimulus currents and determining the impedance of the at least one of the first and second body parts based on the received voltages, wherein the stimulus currents comprise a current signal and a complementary current signal thereby forming a differential current signal (a differential current source 11 provides outputs to 20 and 22 and develops two identical 180 degree out of phase, see Column 3, Line 20 through Column 4, Line 20). Bookspan teaches an impedance apparatus comprising a control module (17, 12-15, see Figure 1). Therefore it would have been obvious to a person of ordinary skill in the art to modify the device taught by Addis to include a main module as taught by Bookspan in order to power and operate the impedance module.

Regarding claim 2, Addiss further teaches the apparatus wherein the impedance module comprises a current generator (20, 22) for generating the stimulus currents, the current generator comprising: a) a first current generation module (54) for generating an internal current signal; b) a first output impedance unit connected to the first current generation module (58) for generating the current signal based on the internal current signal; c) a second current generation (52) module connected to the first current generation module for generating an internal complementary current signal; and, d) a second output impedance unit (56) connected to the second current generation module

for generating the complementary current signal based on the internal complementary current signal.

Regarding claim 6, Addiss/Bookspan teaches the system wherein the impedance module further comprises: a) a processing unit (31) for creating a current control voltage signal for controlling parameters related to the stimulus currents; and, b) a digital-to-analog converter (31) connected to the processing unit for receiving the current control voltage signal and generating an analog current control voltage signal; wherein, the current generator further comprises: c) a single-ended differential conversion unit (R1, D1, D2, R2) connected to the digital-to-analog converter and the first current generation module for converting the analog current control voltage signal to a differential current control voltage signal.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Addiss (US 5,623,938) in view of Bookspan (US 5,086,781) and Dunseath Jr. (US 4,751,471).

Addiss/Bookspan fails to teach the device comprising a first current shield generator for generating a current shield signal related to the current signal; and, b) a second current shield generator for generating a complementary current shield signal related to the complementary current signal; wherein, the current shield signal and complementary current shield signals are provided to the front-end module to shield the current signal and complementary current signal from noise. Dunseath teaches the fundamental inventive concept of providing a current shield generator (Figure 3) for creating a signal to protect an electrode lead wherein the shield is driven at the same

potential as the input signal to minimize noise, (See Column 6, Lines 29-67) and Addiss teaches each signal being 180 degrees out of phase having an opposite voltage. Therefore it would have been obvious to a person of ordinary skill in the art at the time of the invention to include a shield generator as taught by Dunseath for each of the complementary output signals in order to provide shields having a potential which is matched to the input signal in order to minimize noise, see Dunseath Column 6, Line 50-60 by corresponding shield generators as claimed in claim 3.

Claims 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Addiss (US 5,623,938) in view of Bookspan (US 5,086,781) and Davies (US 2003/0216661 A1) and

Addiss further teaches the system, wherein the impedance module comprises: a) a signal conditioning unit (resp circuitry 18) for pre-processing the received voltages to produce a single-ended processed measured voltage, the received voltages forming a differential signal and including a first measured voltage signal and a second measured voltage signal (see Figure 2). Addis fails to teach the device comprising a programmable gain amplifier. Addiss fails to teach a programmable gain amplifier. Davis teaches a programmable gain amplifier (160) in order to properly calibrate a measured signal prior to input into a A/D converter to improve signal resolution. Therefore it would have been obvious to a person of ordinary skill in the art at the time of the invention to include a programmable gain amplifier as taught by Davis in order to

improve the A/D resolution for analysis by a processing unit to for calculating a measured parameter, see Davis [0061].

Claims 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Addiss (US 5,623,938) in view of Bookspan (US 5,086,781) and Davies (US 2003/0216661 A1) and Dunseath Jr. (US 4,751,471).

Addiss/Bookspan fails to teach the device comprising a first current shield generator for generating a current shield signal related to the current signal; and, b) a second current shield generator for generating a complementary current shield signal related to the complementary current signal; wherein, the current shield signal and complementary current shield signals are provided to the front-end module to shield the current signal and complementary current signal from noise. Dunseath teaches the fundamental inventive concept of providing a current shield generator (Figure 3) for creating a signal to protect an electrode lead wherein the shield is driven at the same potential as the input signal to minimize noise, (See Column 6, Lines 29-67) and Addiss teaches each signal being 180 degrees out of phase having an opposite voltage. Therefore it would have been obvious to a person of ordinary skill in the art at the time of the invention to include a shield generator as taught by Dunseath for each of the complementary output signals in order to provide shields having a potential which is matched to the input signal in order to minimize noise, see Dunseath Column 6, Line 50-60, by corresponding shield generators as claimed in claim 12. Regarding claims 13

and 14 Dunseath further teaches the shield generator comprising an amplifier unity gain, see Column 6, Lines 50-67.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See Form 892 for pertinent prior art not relied upon, along with additional information of the references cited in this office action.

Contact Info

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL C. STOUT whose telephone number is (571)270-5045. The examiner can normally be reached on M-F 7:30-5:00 Alternate (Fridays).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Max Hindenburg can be reached on 571-272-4726. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/M. C. S./
Examiner, Art Unit 3736

/Max Hindenburg/
Supervisory Patent Examiner, Art Unit 3736